Chapter 5: MEMS Device Processing

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The growth of MEMS has largely been due to innovations in processing technologies. Adaptations in the processes used to manufacture integrated circuits have led to the development of MEMS and will continue to define the dimensional limitations in devices. It is ultimately these technologies that determine the specifications and reliability characteristics of any given device. As such, they are critically important to understanding MEMS. This chapter offers a brief overview of the most common processing techniques used today. It then describes the integration of these techniques into micromachining.

In the fabrication of common MEMS devices, there are two basic techniques employed. Devices can be constructed by patterning the bulk material of a wafer into a desired structure or, alternatively, by patterning thin films of material deposited on the surface of a wafer. These two processes, respectively called bulk and surface micromachining, are the basis for any MEMS fabrication technology.

I. Microfabrication Processing Steps

There is a variety of processing techniques that are often used in all MEMS processes.[6] The degree to which they are successfully implemented in any given technology determines the viability of the technology. They are listed below to give a basic description of MEMS processing.

A. Thin Film Growth and Deposition

Thin films are an essential building block of semiconductor devices. Surface micromachined devices are constructed entirely out of successive layers of thin films and bulk micromachined devices that employ thin films of silicon dioxide for electrical isolation. There are several common methods for placing thin films on MEMS that are discussed in this section.

i) Spin Casting

In this process, a material is in a solution with a volatile liquid solvent. The solution is poured onto a wafer, which is rotated at high speed. As the liquid spreads over the surface of the wafer, the solvent evaporates, leaving behind a thin film of the solid material, which can be anywhere from .1 to 50 μm thick. Spin casting is useful for depositing organic materials, such as photoresist, as well as inorganic glasses. Spin casting blurs the underlying topography of a

structure, yielding a smooth surface. Spun cast materials are susceptible to severe shrinkage whenever the film coalesces, either from solvent removal or post-bake. This means that spin cast films have an inherently high residual stress. Spin cast films are also less dense and more susceptible to chemical attack than materials deposited by other means.[6]

ii) Evaporation

Another way to place a material in a thin film on a wafer is to evaporate them from a hot source. The evaporation system uses a vacuum chamber, which is pumped down from 10^{-6} to 10^{-7} Torr. A crucible is then heated to flash-evaporate material onto a sample. This process is controlled by a shutter, which limits the amount of time in which the wafer is exposed to the crucible. The thickness of the film is governed by the length of time that the shutter is open and is also a function of the vapor pressure of the material. Thus materials with a high melting point, such as tungsten, require high temperatures to evaporate, which can burn organic films that are on the wafer. Since evaporated films originate from a point source and the vaporized materials travel in a straight path, they suffer from shadowing effects that yield non-uniform thickness and poor step coverage.[6] A second factor affecting the coverage is the surface mobility of the species on the substrate. As a general rule, evaporated films are highly disordered, which causes a large residual stress and limits the thickness of the films.

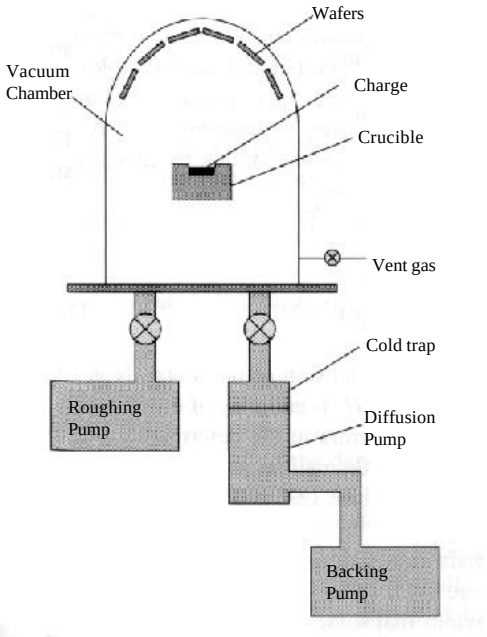

Figure 5-1: A typical evaporation system. (after [46])

iii) Sputtering

Sputtering is a thin film growth technique that eliminates many of the problems inherent to flash-evaporation. Sputtering works by inserting a wafer into a vacuum chamber that is subsequently pumped down to between 10^{-6} and 10^{-8} Torr. Then an inert gas of a few mTorr of pressure is introduced into the system, which is then ignited into a plasma. The highly energetic ions of the plasma strike a target of sample material and tear atoms off its surface. These atoms then form a thin film across the wafer. This process creates a continuous planar flux of the species landing on the wafer, which makes preferable for mass production.[6] Another desirable aspect of sputtering is that the high energy plasma does not have the same temperature problems inherent to evaporation. Most elements and many inorganic and organic compounds can be sputtered. Refractory materials that are difficult to evaporate can be easily sputtered as well. Sputtering can also be done with more than one target, which allows control of the atomic composition of thin film alloys. Sputtered films have better step coverage and uniformity than evaporated films, but they are disorganized structures whose mechanical properties and residual stresses are sensitive to sputtering conditions. Problems also arise from the inert gas used in the sputtering process, which can become trapped in the film and cause inconsistencies in the mechanical properties of the films.[46]

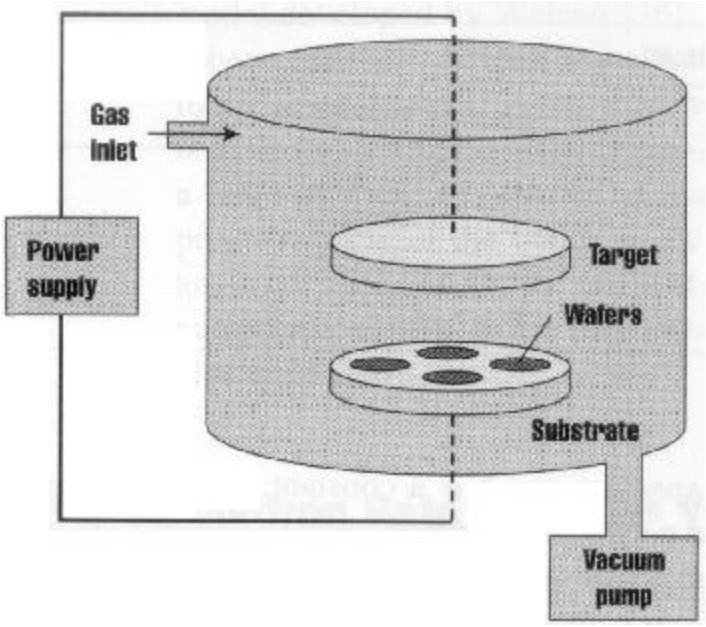

Figure 5-2: Basic sputtering system. (from [46])

iv) Reactive Growth

Reactive growth differs from the previously mentioned methods in that it utilizes chemical reactions with the substrate to construct thin films on wafers. The most common example of this process is with the growth of oxide films on silicon wafers. In this process, a wafer is placed into a furnace with oxygen gas (dry oxidation) or steam (wet oxidation). The silicon is gradually oxidized at a highly predictable rate that depends upon temperature and crystalline orientation.

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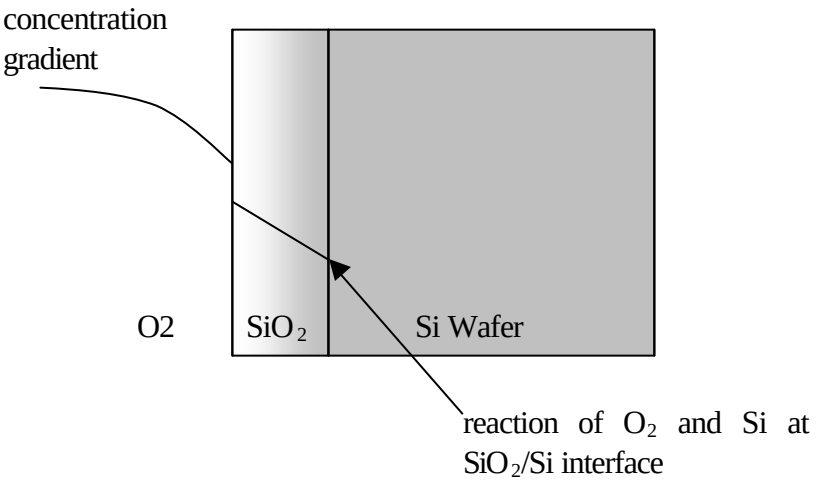

Figure 5-3: Reactive growth process.

Reactively grown films are usually of excellent quality but suffer from large residual stresses due to volume changes in the processed sample. In silicon dioxide growth, there is a volume change of about 45%, which causes mechanical warping.

v) Chemical Vapor Deposition

Chemical vapor deposition, or CVD, involves thermally breaking down gaseous compounds into their components. When they impact a wafer, some of these components nucleate onto it, which grows a thin film. CVD is limited by both the mass transport and reaction-limited processes, with the latter method being preferable due to its better uniformity. This process can be used to deposit many common semiconductor materials, including silicon dioxide, silicon nitride, polycrystalline silicon, and refractory metals. In low pressure thermal CVD, or LPCVD, films with the most desirable mechanical properties are produced. Unlike other methods, CVD films can be deposited conformally on a sample. This property allows CVD films to seal cavities, which can be advantageous in many devices. The stresses and mechanical properties of CVD films can be controlled through the deposition conditions and subsequent annealing. A CVD process called epitaxial growth can be utilized to grow single crystal films on crystalline substrates. Since these films have the same properties as bulk crystals, they could find a multitude of applications in the MEMS industry.

Figure 5-4: A chemical vapor deposition system. (from [179])

vi) Plasma Deposition

Plasma-induced reactions are commonly used for the deposition of MEMS materials. The decomposition of gaseous compounds into reactive species can be induced by the presence of a plasma. This process is known as plasma-enhanced CVD or PECVD. This process utilizes a plasma that contains many ionized species. Some of these species are then deposited on the substrate, which forms a solid film. PECVD films are deposited at a faster rate and require a lower deposition temperature than thermal CVD films, which permits deposition on low-melting point substrates. A number of organic films can also be deposited through PECVD. These films find use as resists for nonplanar substrates. However, PECVD films contain cracks and pinholes. Accurate control of the stoichiometry is difficult as these films contain trapped byproducts from the reaction (especially H_2) that affect the film's mechanical integrity and residual stress.

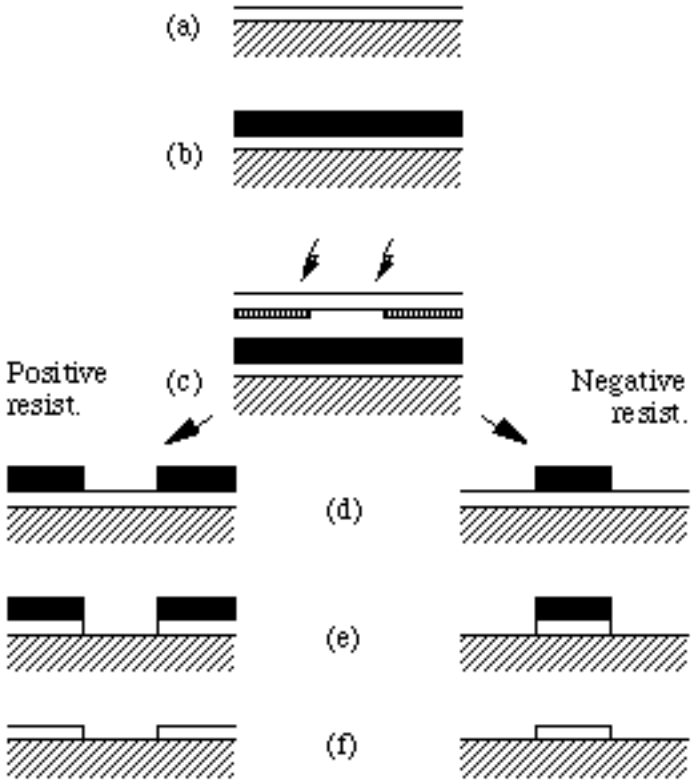

Figure 5-5: The basic photolithographic process in a cross sectional view. First a thin film is deposited on the substrate in (a) followed by the photoresist in (b). UV rays are then focused through a mask onto the surface in (c). Depending upon the type of photoresist, the exposed resist is either removed or left intact in (d). Next, the film is stripped away in places that it is not covered by resist in (e). Finally all of the resist is removed in (f). (from [158])

B. Photolithography

Photolithography is the process by which patterns are transferred onto a wafer. It is accomplished by spinning a thin layer, usually 1 μm thick, of photosensitive organic material, called photoresist, onto the wafer. Then a light source, which typically has an ultraviolet wavelength, is flashed through a computer generated quartz mask and focused onto the photoresist. Then, in a process similar to photographic picture development, the photoresist that has been exposed to light is washed off with the aid of a chemical developer. The remaining resist then acts as a barrier for the underlying regions for further processing. After the processing on the exposed layers has been completed, the resist is washed off and a clean processed wafer is left. This process is typically repeated many times with different mask sets for many of the most common integrated circuits fabrication processes. There are several critical sub-processes in photolithography that need to be addressed as well.

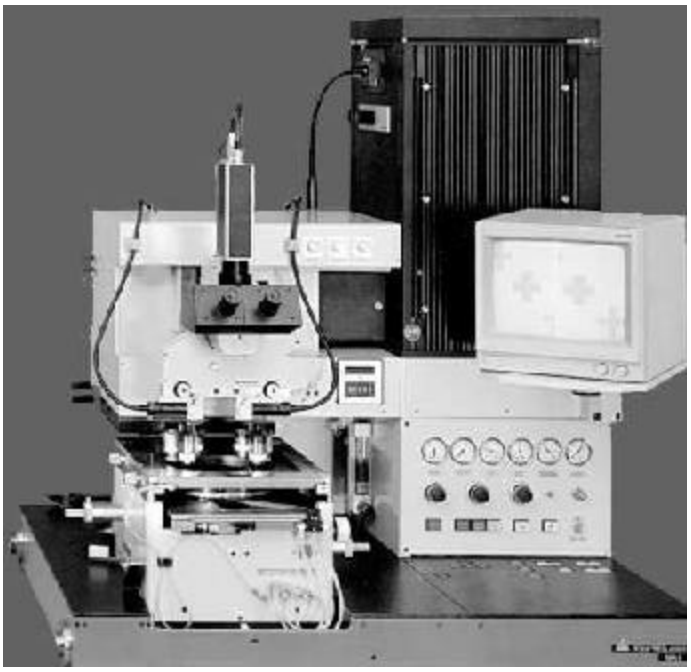

Figure 5-6: Typical alignment machine.

i) Mask Fabrication

The quartz mask is generated by photolithography as well. This process utilizes a glass plate with chromium or emulsion patterns and entails the use of a computerized mask making machine. It starts with a pattern for the mask being entered into the computer through commercially available CAD tools. The pattern is then broken down into small rectangular regions transferred to a mask-making machine. Then a glass plate coated with light blocking chromium or emulsion and photoresist is exposed. The data on the computer is used by the

mask maker to position the mask and determine the size of a variable aperture shutter on the ultraviolet light source. Each of the rectangular boxes is then individually exposed onto the plate. Depending upon the design, this process may be repeated over one hundred thousand times before the mask is finished. After this exposure step, the photoresist is developed and the chromium or emulsion patterns are etched.

ii) Alignment and Exposure

In processes that require multiple masks, each mask layer must perfectly match the features on the substrate. This is done by aligning the mask to special features, called alignment keys, on the wafer prior to exposure. A typical mechanical alignment utilizes a sample, mask holder, a stereoscopic microscope, an ultraviolet light source, and a precision positioning stage, as shown in Figure 5-6. This can either be done with a stepper aligner, which exposes one die at a time, or with a contact aligner, which exposes the whole wafer at once. Often in MEMS, the fabrication process requires photolithography to be performed on both sides of a wafer. To accomplish this, two masks are aligned with each other inside a secure assembly. Then the wafer is inserted and aligned with one of the two masks before being exposed to the ultraviolet light source. There is also an alternative method employed that uses an infrared microscope to locate alignment keys on the back-side, which could offer better alignment precision.[6]

C. Etching and Patterning Techniques

After a pattern has been transferred onto a wafer, it is often necessary to strip away unwanted sections of materials. This process, called etching, determines the dimensions of a MEMS structure. Invariably the reliability of a device will be related to how well the etching is performed and, as such, it must be well understood before a device can be qualified. There are several standard etching techniques used throughout MEMS processing that will be discussed in the following sections.

i) Lift-off

Lift-off is a simple patterning technique. It is accomplished by depositing a layer of sacrificial material, like photoresist, on a substrate. This layer is then patterned, which usually involves the photolithographic processes discussed above. Then a layer of structural film is evaporated onto the substrate. The pattern on the sacrificial layer is then transferred to the structural layer by removing the sacrificial layer. This has the effect of removing all of the structural material that is on top of the sacrificial layer, thus leaving a patterned structural film.

ii) Wet Etching

Wet etching involves immersing a wafer patterned with photoresist or other etch masks in a chemical bath. The chemical etchant selectively removes material not covered with the

mask. The exact profile of the patterning depend on the anisotropy of the etch. Wet etchants all exhibit a degree of isotropic behavior. This has the effect of undercutting the patterned structure, making it smaller than the resist mask. The degree to which the etchants etch the <100>:<110>:<111> directions is responsible for determining the maximum aspect ratio of many structures. Another important aspect of many etchants is their ability to selectively etch one material over the other. Called selectivity, this ratio determines how thick etch stops must be and provides dimensional limits on many technologies.

There are several different chemicals used in wet etching. Acidic etches are used for isotropic release etches. These are usually completely isotropic etches that are designed to separate suspended structures from the underlying substrate. Common acidic etchants are HF, HNO_3, and CH_3COOH. These chemicals etch from 50 to 150 μm/h. SiO_2 is often used as an etch stop for these materials, as it is usually etched at a rate of 2 μm/h.

For an anisotropic etch, alkaline etchants are commonly used. These exhibit different degrees of selectivity and etch rates. Typically these chemicals etch <111> planes much slower than the <100> and <110> planes. This effect and its impact upon MEMS devices is discussed in greater detail in Section 5-IIA. Some etchants can also be influenced by the introduction of boron into the bulk material, which can greatly reduce the etch rate. It is also possible to influence etch rates in a process known as electrochemical etching, which involves applying a voltage across a p-n junction.

iii) Dry Etching

Dry etching, also referred to as reactive ion etching, or RIE, involves using etchants in a gaseous state. The etchant is converted to a highly ionized plasma. Dry etching is performed in a chamber pumped down to a pressure between 10 mTorr and 1 Torr. A wafer is placed between two electrodes, which are then exposed to an RF voltage, which creates a plasma in the chamber. Etching occurs when highly reactive free radicals in the plasma react with the solid-phase material of the film. The anisotropy of the etch is a result of the chemical reaction being preferentially enhanced on the side of the wafer parallel to the electrodes by bombardment from ions in the plasma. The ions impinge the surface of a film and expose underlying material, which is then etched away by the gas. The ions accelerate the etching process considerably, which means that the vertical sidewalls of the wafer, which do not interact with the ions, are not affected by dry etching.

GaAs anisotropic etching is usually performed in chlorinated gasses. One of the problems with GaAs etching is that, due to differences in the etch rates of group III and group V halides, the speed of etching in GaAs varies with crystal planes. In low power, high pressure Cl_2 gasses, significant faceting can occur. There are several methods that can be used to avoid this problem. It is possible to add certain compounds to form polymers in the plasma and passivate the side walls, thus preventing the problem. Another possibility is to use hydrides to

etch arsenic and methane to etch gallium. A mixture of AsH_3 and between 5 to 25% methane has been shown to be an effective anisotropic etchant.[46]

One of the major drawbacks to reactive ion etching is residual damage caused by the etch. With ion fluxes of 10^{15} ions/cm^2 delivered at 300 to 700 eV, substrate damage and chemical contamination are serious issues to consider. Another problem is gas phase particle deposition and metallic impurities originating from the RIE chamber and electrodes. Several more complex techniques have been derived to remove these problems, but they come at added expense and preparation time. It is also known that the RIE can drive impurities into the bulk material to depths of 30 nm, which can limit the fracture strength of a structure.[46]

II. MEMS Fabrication Processes

A. Bulk Micromachining

The distinguishing characteristic of bulk micromachining is that it fabricates micromachined devices out of the bulk of a substrate. In recent years, several variants of this procedure have appeared that utilize different etching and patterning techniques. In this section, a brief overview on bulk micromachining will be offered that will include the most prevalent processing techniques.

Bulk micromachining begins with a single crystal substrate. A thin film of material that is inert to the chemical etchants is then deposited on the substrate. For silicon substrates, silicon oxide or nitride are most commonly used as an etch mask. Then the film is patterned so that the undesired portions of the film are removed. This leaves the bare substrate exposed.

At this point, the bulk material is etched. The etching of the bulk material can either be performed with a wet or a dry chemical etchant. Since the processes associated with these etches are substantively distinct, they will be individually addressed.

i) Bulk Micromachining with a Wet Etch

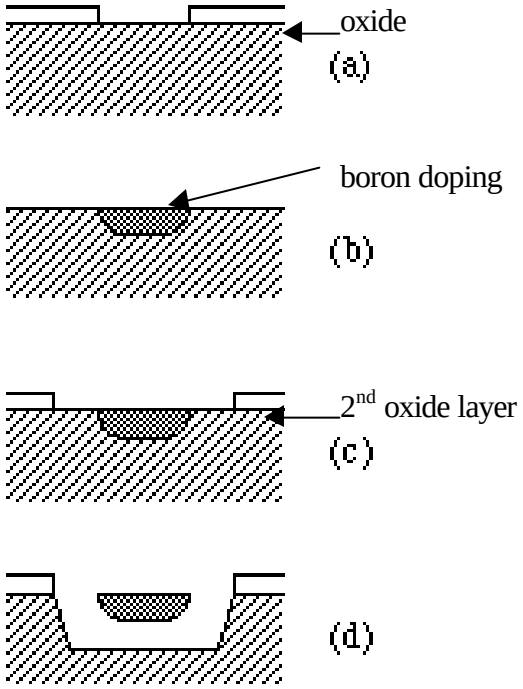

Figure 5-7: A side view of a generic bulk micromachining process. (a) an oxide layer is grown and patterned on top of a <100> silicon wafer. (b) Boron is ion implanted and annealed to the suitable depth. (c) a second oxide layer is grown and patterned. (d) KOH anisotropic etch.

The process associated with the wet chemical etching of silicon is illustrated in Figure 5-7. As the figure shows, this anisotropic etch occurs in diagonal direction. This is a common feature of wet anisotropic etches. Since the early 1960s, alkaline solutions have been used to etch silicon along crystalline planes. The etch rate is slowest in the <111> direction and fastest in the <100> and <110> directions. The result of this uneven etch rate is that the bulk material is etched at an angle of 54.74°, which is the angle between the (100) surface and the four {111} planes. The ratio between the etching in the desired directions and the etching in the undesirable directions is defined as the selectivity. An etchant that has a better selectivity will yield a more defined, and hence better, finished structure.

There are several characteristics of anisotropic etches that lead to important design considerations. The major constraint is that designed features must be bound by the {111} planes thus the resulting structures are necessarily rectangular, with sidewalls sloping away at 54.74^{o}. The use of less popular <110> oriented Si wafers yields vertical sidewalls but the planar features can only be long parallel strips on the substrate, which have limited use. In recent years a number of groups have begun exploring dry etching processes that offer the possibility of anisotropic etchings.

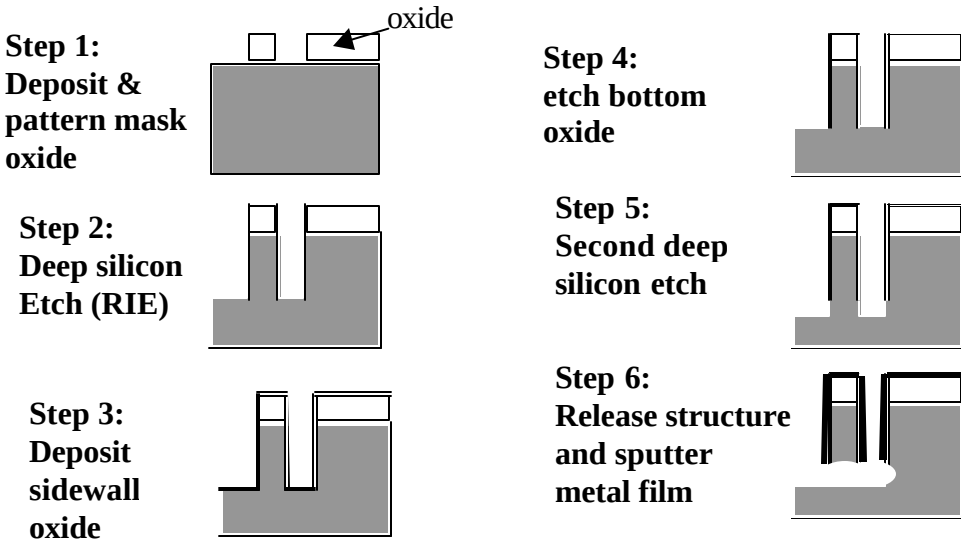

Figure 5-8: A side view of one of the dry etch micromachining processes. In Step 1, an oxide coating is grown on top of the substrate and patterned. Then, in Step 2, a reactive ion etch removes silicon and transfers the pattern from the oxide. Step 4 exposes the bottom of the wafer for Step 5, etches a small amount of substrate. This allows Step 6 to proceed, which is an anisotropic etch that releases that structure from the substrate and often deposits a layer of metallization to create an conductive surface.

ii) Bulk Micromachining with a Dry Etch

Bulk micromachining involving dry etching is performed in much the same way as bulk micromachining with a wet etch. One example of a dry etching process is the SCREAM process, which was developed at Cornell under the supervision of Noel MacDonald and is illustrated in Figure 5-8. This process is conducted by transferring a pattern onto the substrate. Then, a reactive ion etch is performed. Normally after this, a second deep etch is performed to expose oxide-free silicon. From this point, an isotropic etch can be performed to release the whole structure, which creates high aspect ratio structures suspended above the substrate.[180]

There are multiple methods employed to produce finished devices through a reactive ion etch. While the processes vary by research group, all employ a deep reactive ion etch that can create aspect ratios higher than 20:1. It is the ability to produce these high aspect ratio structures, which can have higher mass and capacitance per silicon surface area than many other MEMS technologies, that has helped to drive the development of RIE in MEMS production.

In the production of bulk micromachined devices, it has proven useful to layer devices. The most common method of achieving layered bulk micromachined devices is by bonding two wafers together. For this reason, different wafer bonding techniques will be addressed.

iii) Wafer Bonding

Wafer bonding has been used in recent years for both sealing microsensors and for the construction of composite sensors. There are several kinds of wafer bonding techniques commonly employed, which are discussed below.

(1) Anodic Bonding

Anodic, or electrostatic, bonding is a process that bonds a conductive substrate, which is usually silicon, to a sodium rich glass substrate. This is done by putting the two substrates into direct contact. They are then heated to between 350-400 °C, which mobilizes the sodium ions in the glass. Then a voltage of 400-700 V is applied between the two substrates, with the glass substrate being made negative with respect to the silicon wafer. This repels the sodium ions from the interface and creates an ion-depletion region about a micron thick with electric fields on the order of 7×10^6 V/m. This creates an electrostatic pressure of several atmospheres, which pulls the two wafers together while a thin layer of SiO_2 is formed. The end result of this process is a hermetically sealed bond with a strength that exceeds that of the individual substrates.

There are several reliability concerns in producing these bonds. The high temperature at which the bond is formed can induce thermal mismatch warping in a processed device. There can also be warping at the bonding interface from unmatched thermal coefficients of expansion. Currently, Corning glass 7740 offers the closest match to silicon. Another concern is the introduction of the large voltages and electric fields inherent to the bonding process. It is possible to destroy the device in the bonding process if these factors are not considered.[6]

(2) Low-Temperature Glass Bonding

Low-temperature glass bonding offers a viable alternative to anodic bonding for applications where high voltages are unacceptable. In this process, the bonding interface is covered with a thin film of low-temperature glass. The wafers are then placed into contact under pressure and heated to create the bond. The low-temperature glass then either melts or crystallizes, depending upon the actual glass used, which bonds the two substrates. In general, these bonds are not as strong, and thus less reliable, as anodic bonds.

In some applications, glass frits are used to form bonds. These frits are solutions of metal oxides that form a paste. Under pressure, the frit will form a film that seals rough surfaces. This film can be hardened by heating it to between 300-600°C. The thermal expansion coefficient of these frits can range between two to five times more than that of silicon, which can lead to warping problems.

(3) Fusion Bonding

Fusion bonding is a technique that fuses two materials together through high temperature. This process is used commonly in the production of silicon-on-insulator devices and pressure sensors. It is accomplished by taking two clean wafers and placing them on top of one another. This bonds the two wafers through Van der Waals forces. They are then placed into a furnace to create the final bond at temperatures in excess of 1000 ^{o}C.

While this process creates strong bonds it has some serious drawbacks. High furnace temperatures prohibit the use of active devices in the wafer prior to bonding. Furthermore, the weak initial bond makes the final bond strength very sensitive to the surface topology of the wafers and the presence of contaminants. For these reasons, these bonds are not always the most reliable and are often difficult to use.

iv) Reliability Issues

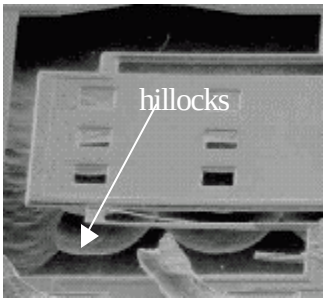

Figure 5-9: Hillocks caused by wet etchants.

Bulk micromachined devices have reliability concerns that vary with the processes used to fabricate them. One problem with using wet etchants is that they create sharp corners in silicon. These corners are natural stress concentration points that will weaken the strength of a structure. The use of chemical etchants can also lead to rough features on the surfaces of processed structures. The features, called hillocks in the literature, are a periodic undulation in the silicon. The presence of hillocks, which has been measured as high at 10μm, precludes many electrostatic devices from operating properly. Furthermore, hillocks create natural stress concentation points that are more likely to fragment over time, which can create destructive free particulates in the MEMS device.

Dry etching can have reliability problems caused by the reactive ion etch. While the sidewalls created by these etches are intended to be vertical, they often have irregular features. Poor control over the conditions inside the etching machine can lead to unintended geometric effects on finished devices, as shown in Figure 5-10. A study conducted at Carnegie-Mellon University[168] has shown that the O_2 flow rate, pressure, and RF power density of the RIE machine can influence the formation of different sidewall features. Devices produced that have these uneven sidewall features will have questionable reliability characteristics, as these features are indicative of a poorly controlled process line. Devices with these features will also depart from predicted operational characteristics and, as a result, devices made with dry etches need to

be screened for these characteristics. One positive feature of using an RIE system is that it produces more rounded corners than wet etching. As a result, these structures are not as prone to fracturing as wet etched devices.

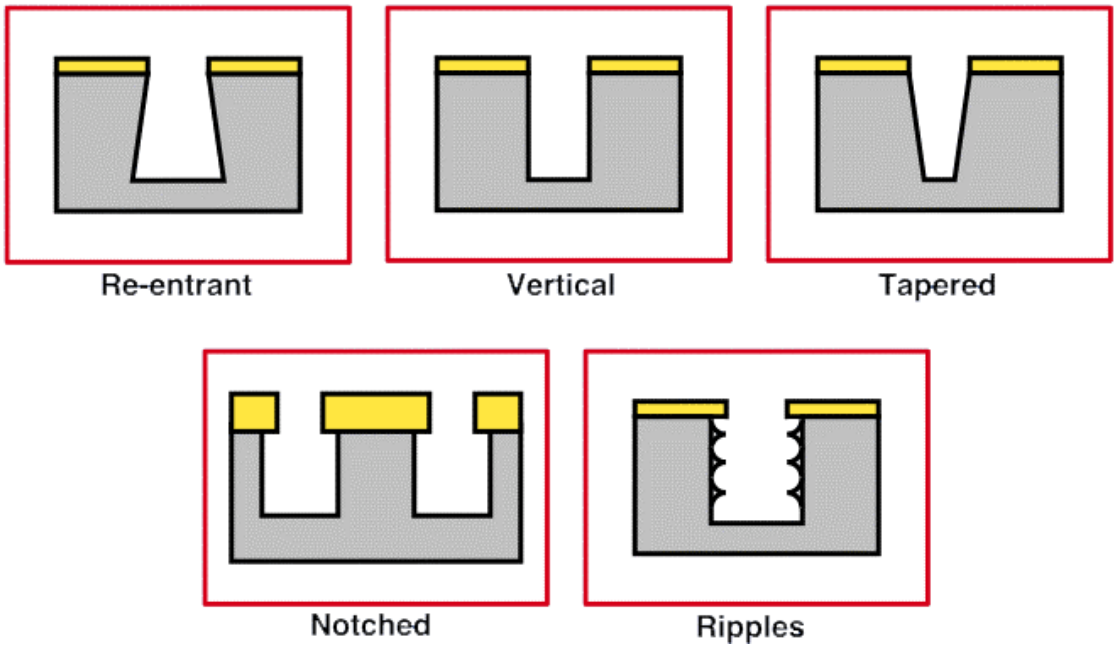

Figure 5-10: Possible sidewall features created by a poorly controlled RIE. (from [181])

B. Surface Micromachining

Surface micromachining is a process that offers many advantages and disadvantages different from bulk micromachining. Surface micromachining differs from bulk processes in that devices are fabricated entirely out of thin film materials. One of the most attractive features of this process is that it, like reactive ion etching, does not suffer from the 54.7° feature enlargement common to bulk micromachining with wet etchants. A key design feature of surface micromachining is the choice of structural and sacrificial thin films.

A typical surface micromachining process starts with a silicon substrate passivated by silicon nitride. Upon this substrate, a thin film of sacrificial oxide is deposited. This film is then patterned according to the device's design. After this, a layer of thin film polysilicon is deposited to form the structural material. The most common method of deposition is through LPCVD, which can either produce polycrystalline or amorphous silicon films depending upon reaction temperature. This process allows tight control over the residual stress in the films. After this, the oxide layer is often removed by immersing the structure in a HF solution. For most surface micromachining, the process of depositing a layer of oxide, followed by a layer of polysilicon will be repeated several times to produce multi-layered structures. Figure 5-11 shows a common process developed by MCNC that uses three layers of polysilicon.[144]

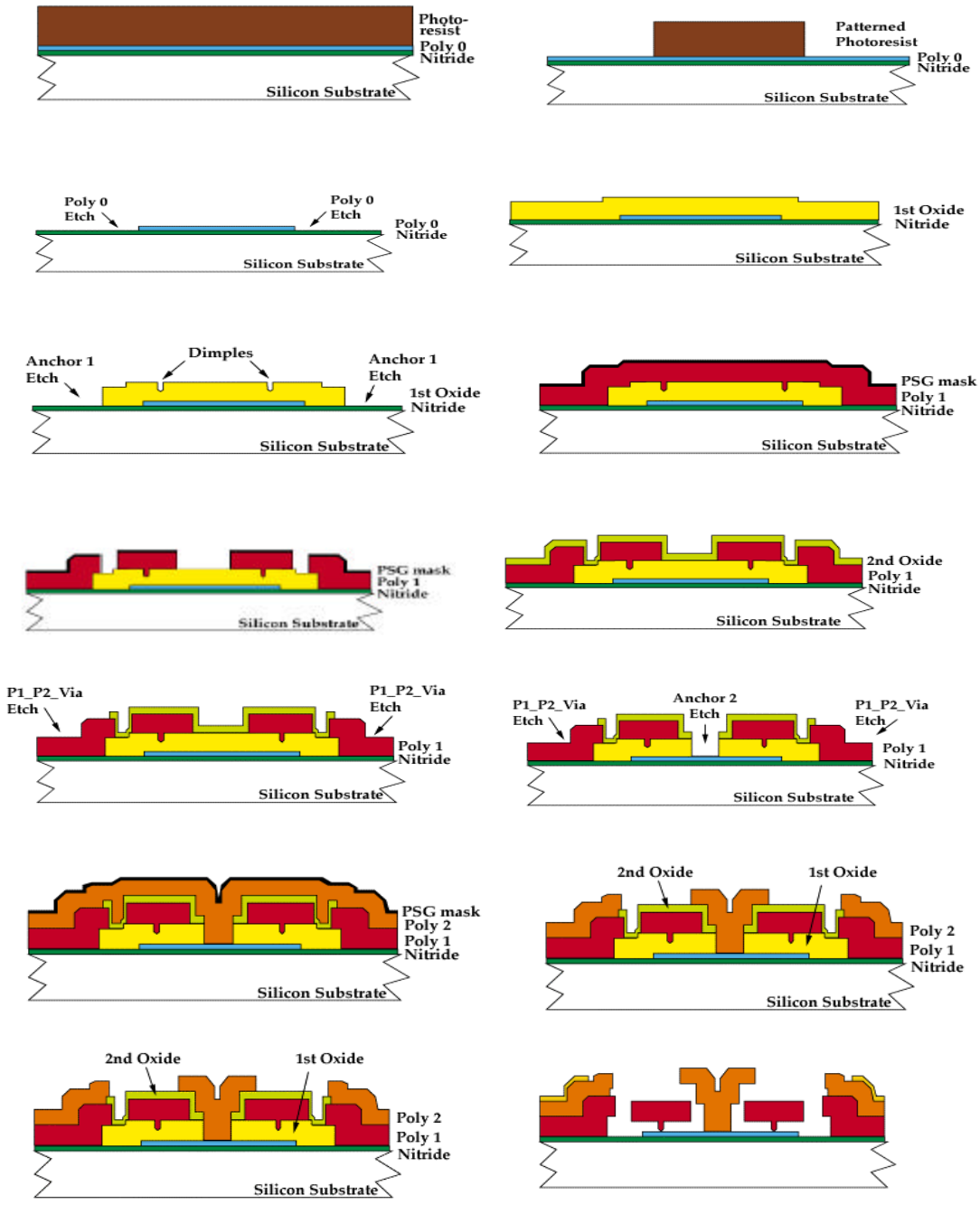

Figure 5-11: The surface micromachining process using three layers of polysilicon. (from [144])

The ability to layer structures in surface micromachining has piqued the interests of many researchers. It allows for the construction of structurally complex sensors that are difficult to fabricate with bulk processes.

i) Reliability Issues

Another consideration that needs to be addressed in these devices relates to their mechanical properties. While bulk materials have well understood properties, the mechanical attributes of surface micromachined devices depend upon thin film processing conditions. To ensure reproducible devices, these conditions must be well controlled. In particular, many of the materials used in these devices have large built-in stresses which affect the performance of the device to a variable degree (Figure 5-12).

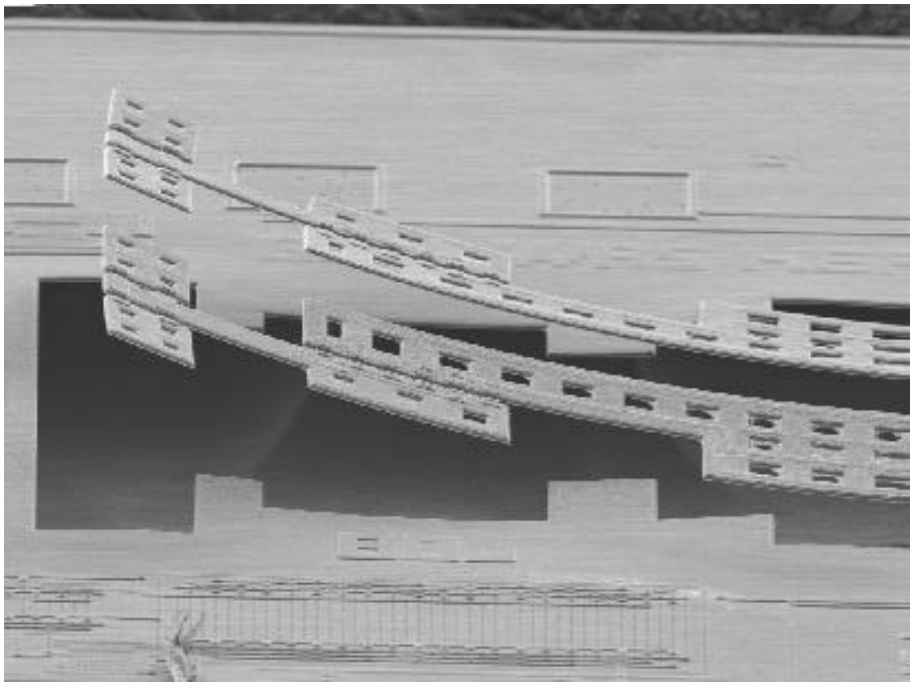

Figure 5-12: MEMS structure with a large residual stress. (from JPL)

Surface micromachined devices also have adhesion problems that are inherently worse than bulk micromachining. Cantilever beams are produced in surface micromachining on top of a sacrificial oxide layer, which is removed by immersion in an HF bath. Then the structure is cleaned in de-ionized water. After this, a of 5-30Å thick oxide layer will form on the surface of the polysilicon. There will also be hydroxyl groups in the oxide layer, which have a high surface energy. This makes the oxide layer extremely hydrophilic, which creates a strong capillary force between the beams and the substrate. This capillary force will pull the beam to the substrate and create an adhesive bond between the beam and the substrate.

There are several methods now used to prevent released structures from bonding to the substrate. Several groups, including those led by R. Howe at Berkeley and N. Tien at Cornell, utilize a thin film of self assembled monolayers on the surface micromachined device. The monolayers are hydrophobic, which creates a repulsive force between the substrate and the suspended structures, which effectively prohibits adhesive bonds from forming. However, it remains unclear what impact the monolayers will have on the long term reliability of these devices. Another method that prevents the creation of adhesive bonds involves using polyimide as a sacrificial material. This technique, developed by Gregory Kovacs at Stanford University, utilizes aluminum structures that are released in an oxygen gas. Since this process does not utilize any liquids, no adhesive bonds are formed.

C. LIGA

LIGA is a German acronym that stands for lithography, electroplating, and molding. LIGA was developed to produce high aspect ratio structures. LIGA offers some unique properties that makes it an interesting technology. LIGA enables the construction of structures with the thickness of bulk micromachining with a degree of design freedom similar to surface micromachined devices. This technology offers structures several hundred microns thick, with a minimum feature size of only a few microns.

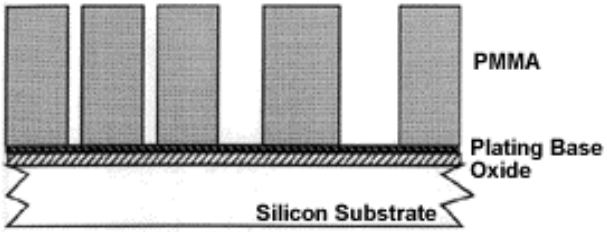

Fig. 1 Fabrication is done on a (100) silicon wafer with a 0.5μm oxide layer. A plating base is formed by sputtering 300nm of Ti and 5000A of Cu with a top layer of 300A Ti. The Ti and Cu also act as a release layer. Thick photoresist is applied and exposed using x-rays from a synchotron and developed with a solvent.

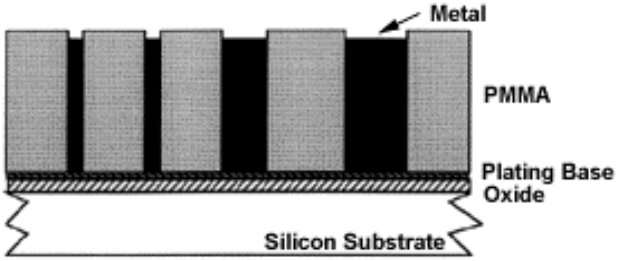

Fig. 2 The desired metal, in this case nickel, is electroplated onto the substrate, filling the voids in the PMMA.

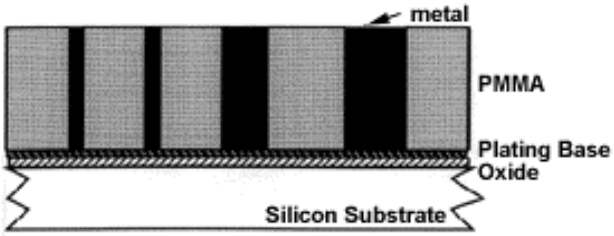

Fig. 3 The metal and PMMA are milled back to produce a uniform top surface.

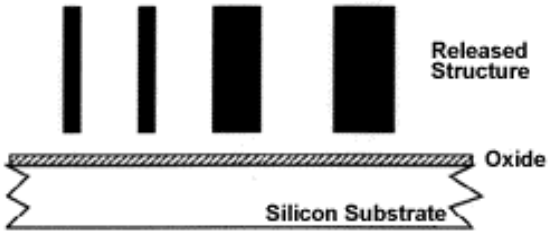

Fig. 4 Finally, the PMMA is removed. If desired, the customer can release the structures from the substrate by etching away the plating base in an NH_4O_2/H_2O_2 solution.

Figure 5-13: The basic LIGA process. (from [144])

The LIGA process begins by depositing a layer of thick photoresist, usually poly-methyl methacrylate, or PMMA, that is between 300 and 500 μm thick onto a conductive substrate. The PMMA is then patterned with short wavelength radiation from an X-ray synchrotron source

for several hours. Then a layer of metal is electroplated onto the exposed area of the conductive base plate, which fills in the open areas created by the patterning. Then the metal structure is separated from the PMMA mold, as shown in Figure 5-13. This metal structure can in turn be used as a mold insert for injection molding to form multiple plastic replicas of the original plating base. These plastic replicas can then be used to make multiple copies of the original structure.

The LIGA technique involves some advances beyond semiconductor processing. The X-ray source must be capable of delivering at least 1 GeV of energy at wavelengths shorter than 7 Å. To withstand this bombardment, the opaque part of the mask must be constructed out of a material with a high atomic number. Furthermore, the transparent part of the mask must have a low atomic number to allow the photons to pass through without heavy absorption and scattering. Successful masks have been made with 3 μm thick gold in the opaque region and 1 to 2 μm thick silicon nitride or titanium foil in the transparent region. Another hurdle to overcome is the electroplating of the patterned structure. This step requires accurate controlling of current density, temperature, concentration, and composition of the plating solution to prevent the formation of hydrogen bubbles, which can ruin a structure. These conditions also determine the internal stress of the device and thus must be well understood and controlled to ensure reliable device operation.

i) Reliability Issues

LIGA, as a relatively costly technology, has not been researched as fully as other MEMS processes. As a result, the LIGA process can have great variability across process runs. Another problem with LIGA is that the injection molding process and mold separation processes require almost perfectly vertical structures. This issue has become a strong factor in the device yield of LIGA technology.

D. GaAs Processing

The processing of gallium arsenide can be as varied as silicon processing. While there are many GaAs processes that are very similar to those of silicon, there are some techniques that are unique to GaAs. These GaAs processing techniques are an offshoot of bulk micromachining that utilizes the unique properties of GaAs and its ternary alloy AlGaAs to produce structures.

One method of processing GaAs wafers is to use ion implantation. The first step is to layer an implantation mask. Then a layer of N ions is implanted into the substrate. The depth that they travel into the substrate is a function of accelerating voltage. Then the mask is removed and the sample is annealed at 750°C for about 30 minutes while covered with PECVD Si_3N_4. This process recrystalizes the buried layer to a $GaAs_{1-x}N_x$ layer. Then a SiO_2 etch mask is evaporated onto the surface of the wafer. Then an anisotropic etch is performed to expose the

buried layer. Finally a selective etch is used to remove the buried layer. This process is illustrated in Figure 5-14.

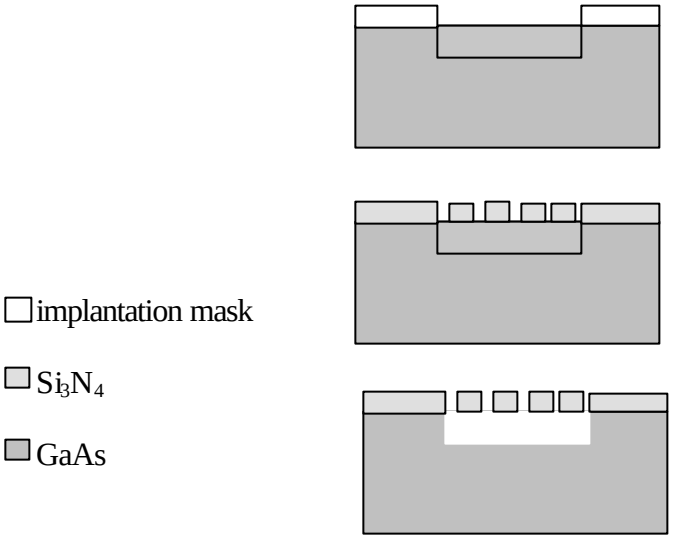

Figure 5-14: Fabrication of a suspended structure in GaAs. First a layer of N ions is implanted into the substrate, then a Si_3N_4 structure is patterned on top. Finally the N ion layer is selectively removed, leaving a suspended structure.

Another GaAs process used in producing microstructures is to micromachine through the use of epitaxy. This process utilizes the chemical difference between GaAs and $Al_xGa_{1-x}As$ in order to gain the desired results. The first step to this process is to use epitaxial growth to produce an undoped $Al_xGa_{1-x}As$ layer on top of a GaAs wafer. Then a Si_3N_4 etch mask is applied to the back side of the wafer. This mask then allows the full removal of the GaAs by using an H_2O_2/NH_4OH solution, which leaves only a thin membrane of $Al_xGa_{1-x}As$ as shown in Figure 5-14.[21]

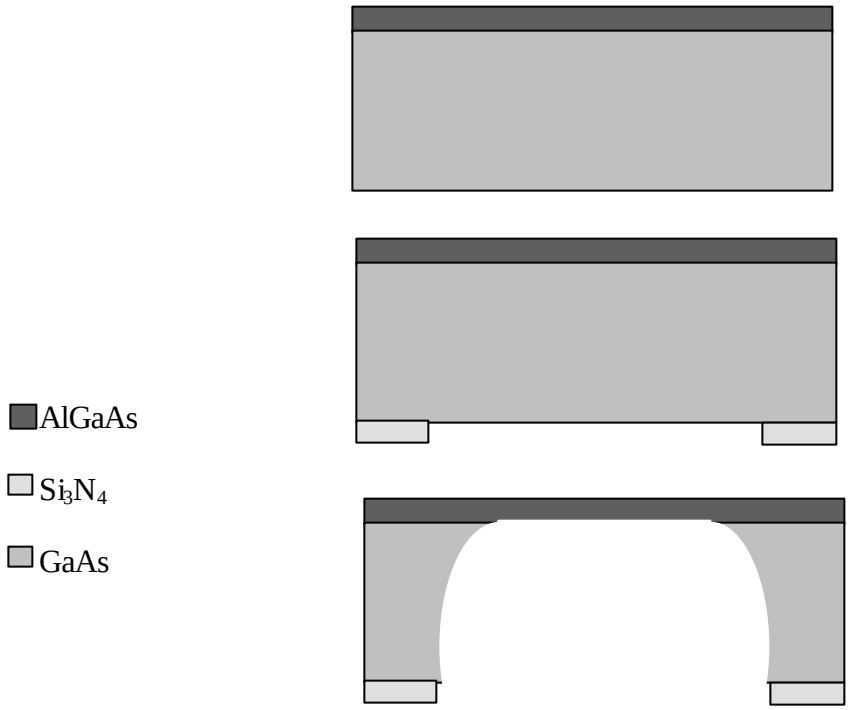

Figure 5-15: Fabrication of an AlGaAs membrane. The first step in this process is to epitaxially grow a AlGaAs layer on the GaAs substrate. Then a Si_3N_4 etch mask is used to etch away the back side of the structure.

i) Reliability Issues

One issue that is an area of concern in GaAs processing is the internal film stresses created by thermal mismatch in GaAs-$Al_xGa_{1-x}As$ heterostructures. Epitaxial growth is a high temperature process which will, even though the lattice parameters of these two compounds are well matched, create a strain from differing expansion coefficients.

III. Additional Reading

Sze, S. M. ed., Semiconductor Sensors, Wiley Inter-Science, New York, 1994.

S. A. Campbell, The Science and Engineering of Microelectronic Fabrication, Oxford University Press, Oxford, 1996.